Semester: 2	
Programme : B.Sc. Computer Science (Hons)	
Course : COMPUTER SYSTEM ORGANISATION	
Paper code: C1CS230222T / C1CS230222P	**Credits: 4**
Hours/week : Theory: 3 / Practical 2	
Category: Core/MDC/SEC/VAC : Core	
Theory / Practical / Composite : Composite	
No of Modules : 1	

Course Overview: This course provides a foundational understanding of computer system architecture from the hardware-software interface perspective. Students explore how high-level programs are executed by underlying hardware components—processors, memory, and I/O subsystems—through instruction sets, data paths, and control mechanisms. The curriculum bridges theoretical concepts (e.g., Von Neumann architecture) with practical implementation details (e.g., ALU design, cache mapping), enabling students to reason about performance, efficiency, and design trade-offs in real computing systems.

Course Outcome:

1. **Explain** the structure of instruction sets, addressing modes, and architectural models, and **analyze** their impact on program execution efficiency.
2. **Design** memory interfaces using multiplexers/tri-state devices and **evaluate** trade-offs in memory hierarchy organizations (cache mapping, virtual memory) for performance optimization.
3. **Compare** hardwired and microprogrammed control unit implementations and **assess** microinstruction parallelism techniques for control signal generation.
4. **Differentiate** I/O techniques (polling, interrupts, DMA) and **configure** bus protocols (handshaking, arbitration) to minimize CPU overhead in data transfer operations.
5. **Implement** fixed- and floating-point arithmetic algorithms (including Booth's multiplication) and **construct** a combinational ALU circuit for fundamental arithmetic/logic operations.

Prerequisites:

- Digital Logic Design / Boolean Algebra
- Programming Fundamentals
- Basic understanding of algorithms and data representation

SYLLABUS

UNIT/Module	CONTENT	HOURS or NUMBER OF CLASSES	CO Mapping	COGNITIVE LEVEL
I.	**Instruction:** Operation Code and Operand. Zero, One, Two and Three address instruction. Instruction types, Addressing modes.	**5**	**CO1**	**Understand, Apply (K2, K3)**
II.	**Memory:** Memory Organisation - Interfacing with system bus using multiplexers/tri-state devices, Types of Memory. Memory Hierarchy, Associative Memory, Cache Memory, Virtual Memory.	**12**	**CO2**	**Apply, Evaluate (K3, K5)**

III.	Von Neumann vs Harvard Architecture	**1**	**CO1**	**Understand, Apply (K2, K3)**
IV.	**Control Unit:** Control Structure and Behaviour, Hardwired Control and Micro programmed Control: Parallelism in Microinstruction	**7**	**CO3**	**Analyze, Evaluate (K3, K5)**
V.	**I/O Organisation:** Polling, Interrupts, DMA, I/O Bus Interfacing and Protocols - Strobe Control, Handshaking, Bus Arbitration.	**6**	**CO4**	**Understand, Apply (K2, K3)**
VI.	**Fixed and Floating Point Arithmetic:** Addition, Subtraction, Multiplication (Booth's Algorithm) & Division.	**4**	**CO5**	**Apply, Create (K3, K6)**
VII.	**ALU:** Combinational ALU Design	**4**	**CO5**	**Apply, Create (K3, K6)**

Text Books

1. **1.** Digital Computer Electronics, Malvino and Brown, Tata McGraw-Hill
2. **2.** M. Mano, Computer System Architecture, Pearson Education 1992
3. **3.** W. Stallings, Computer Organization and Architecture Designing for Performance, 8th Edition, Prentice Hall of India,2009
4. 4. Carl Hamacher, Computer Organization, Fifth edition, McGrawHill, 2012.
5. 5. Computer Architecture and Organization, Hayes, McGraw-Hill
6. 6. Computer Organization and Design, P. Pal Chaudhuri, Prentice-Hall of India

Evaluation

Theory CIA: 12 Attendance: 3 Semester Exam: 45	Practical CA: 38 Attendance: 2

Paper Structure for Theory Semester Exam Module: Answer 3 out of 5 of 15 marks each

Course outcomes (COs) and Cognitive Level Mapping

COs	CO Description	Cognitive levels
CO1	Explain the structure of instruction sets, addressing modes, and architectural models, and analyze their impact on program execution efficiency.	Understand → Analyze (K2, K3)
CO2	Design memory interfaces using multiplexers/tri-state devices and evaluate trade-offs in memory hierarchy organizations (cache mapping, virtual memory) for performance optimization.	Apply → Evaluate (K3, K5)
CO3	Compare hardwired and microprogrammed control unit implementations and assess microinstruction parallelism techniques for control signal generation.	Analyze → Evaluate (K3, K5)
CO4	Differentiate I/O techniques (polling, interrupts, DMA) and configure bus protocols (handshaking, arbitration) to minimize CPU overhead in data transfer operations.	Understand → Apply (K2, K3)

CO5	Implement fixed- and floating-point arithmetic algorithms (including Booth's multiplication) and construct a combinational ALU circuit for fundamental arithmetic/logic operations.	Apply → Create (K3, K6)